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PTO/SB/21 (09-04)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/617,980
Filing Date	7/10/2003
First Named Inventor	Edward A Ramsden
Art Unit	2819
Examiner Name	Daniel D Chang
Attorney Docket Number	M-15145 US

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☑ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):
  Request for Certificate of Correction

Remarks

Certificate NOV 25 2005 of Correction

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Lattice Semiconductor Corporation		
Signature	Mark L Becker		
Printed name	Mark L Becker		
Date	11/18/05	Reg. No.	31325

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Mark L Becker		
Typed or printed name	Mark L Becker	Date	11/18/05

PTO/SB/80 (04-05)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 29416

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 29416

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

Lattice Semiconductor Corporation
5555 NE Moore Court
Hillsboro, OR 971247-6421

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Martin R. Baker	Date	June 30, 2005
Name	Martin R. Baker	Telephone	503-268-8000
Title	Vice President & General Counsel		

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (09-04)
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Edward A Ramsden

Application No./Patent No.: 6,958,625 B1 Filed/Issue Date: 10/25/2005

Entitled: PROGRAMMABLE LOGIC DEVICE WITH HARDWIRED MICROSEQUENCER

Lattice Semiconductor Corporation, a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☑ the assignee of the entire right, title, and interest; or

2. ☐ an assignee of less than the entire right, title and interest.
The extent (by percentage) of its ownership interest is_____ %

in the patent application/patent identified above by virtue of either:

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 015217, Frame 0919, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

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☐ Additional documents in the chain of title are listed on a supplemental sheet.

☐ Copies of assignments or other documents in the chain of title are attached.
[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

_____ 11/18/05
Signature Date

Mark L Becker 503-268-8629
Printed or Typed Name Telephone Number

Associate General Counsel, IP
Title

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent No.:	6,958,625 B1
Issued:	October 25, 2004
First Named Inventor:	Edward A Ramsden
Title	PROGRAMMABLE LOGIC DEVICE WITH HARDWIRED MICROSEQUENCER

REQUEST FOR EXPEDITED ISSUANCE OF CERTIFICATE OF CORRECTION PURSUANT TO 37 CFR 1.322

Certificate of Corrections Branch
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Review of the above-identified patent has revealed errors in the patent attributable solely to the Patent and Trademark Office. Applicant therefore requests that a Certificate Of Correction be issued to correct these errors.

The location of the errors in the patent and the corresponding correct language in the application file are set forth below:

Error in Patent	Correct Language in Application File
Col. 6, line 61 (claim 11)	Amendment filed 2/23/05, claim 11, lines 1-2

Documentation supporting this request and a form PTO/SB/44 showing the corrections are enclosed.

Although no fees are believed due, the Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 501958.

Respectfully submitted,

Date: 11/18/05

By: _____

Mark L Becker
Associate General Counsel, IP
Reg. No. 31,325
Customer No. 29416

Lattice Semiconductor Corporation
5555 NE Moore Court
Hillsboro, OR 97124
Phone: 503-268-8629
Fax: 503-268-8077

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,958,625 B1

APPLICATION NO.: 10/617,980

ISSUE DATE : October 25, 2005

INVENTOR(S) : Edward A. Ramsden

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 11, line 61: "executing co the" should read -- executing the --.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Lattice Semiconductor Corporation
5555 NE Moore Ct., Hillsboro, OR 97124

NOV 2 8 2005

appropriate microinstruction which may arbitrarily be denoted to correspond to a state SQ. Microsequencer **40** may then sequence or jump through any number of states. These states may be arbitrarily denoted as states SQ through SZ. For these states, however, the executed microinstructions from microsequencer **40** would all have this "power bad suppressor" input within field **320** set to true, thereby permitting normal operation of the power bad flag.

As described above, macrocells **30** may be configured to operate either sequentially or combinatorially. Should macrocells **30** be configured for combinatorial operation, they provide no memory functionality. Thus, in such combinatorial operation, microsequencer **40** provides the sole means for storing the current state of the desired finite state machine. Should macrocells **30** be configured for sequential operation, they may be used to store secondary state information as desired by a user.

Consider the advantages of the microsequencer architecture disclosed herein. The sequential actions for the desired finite state machine may be controlled by the sequential bit patterns output through the microsequencer's auxiliary command **45**. By processing auxiliary command **45** in conjunction with inputs **15**, logic block **10** allows single-cycle conditional branches to be made on complex Boolean conditions (e.g. X AND (Y OR NOT Z), where X,Y, and Z are included within inputs **15**. This results in a language with the following statements:

OUTPUT VARIABLE1=TRUE|FALSE,

VARIABLE2=TRUE|FALSE, . . .

IF<boolean_expression>GOTO STEP XXX

The ability to branch on the outcome of a complex and arbitrary boolean expression is a capability provided by the microsequencer architecture disclosed herein. Such a capability is not normally provided by a traditional microsequencer, where branching decisions are based on the status of one or more bits, and complex boolean conditions must be evaluated in multiple cycles. Rather than use multiple cycles, the complex expressions are evaluated in one clock cycle by logic block **10**, and the resulting single boolean result is used to control the microsequencer's decision to jump or not to jump.

The above-described embodiments of the present invention are merely meant to be illustrative and not limiting. Various changes and modifications may be made to the embodiment without departing from the principles of this invention. For example, although microsequencer **40** has been described as performing the sequencing for a programmable-AND-array-based logic block, it will be appreciated that microsequencer **40** may receive its input conditions from other types of logic blocks such as lookup-table-based logic blocks. Accordingly, the appended claims encompass all such changes and modifications as fall within the true spirit and scope of this invention.

What is claimed is:

1. A programmable logic device comprising;

a programmable logic block including a plurality of macrocells, the macrocells operable to provide logical outputs at the block's output terminals from logical inputs received at the block's input terminals; and

a hardwired microsequencer coupled to the input and output terminals of the programmable logic block, the microsequencer operable to provide a sequence of logical inputs to the programmable logic block, at least part of the sequence determined by logical outputs provided by the macrocells of the programmable logic block.

2. The programmable logic device of claim **1**, wherein the programmable logic block comprises a programmable AND array configured to provide a plurality of product terms based upon a set of logical inputs, and wherein the plurality of macrocells are operable to generate the logical outputs from the product terms.

3. The programmable logic device of claim **1**, wherein the part of the set of logical inputs provided to the programmable logic block by the microsequencer are derived from microinstructions executed by the microsequencer.

4. The programmable logic device of claim **2**, wherein the microinstructions include an input, a jump destination, and a select command.

5. The programmable logic device of claim **1**, wherein the microsequencer includes:

a memory configured to store a set of microinstructions that include at least some of the logical inputs provided to the programmable logic block; and

a program counter coupled to the memory and configured to provide addresses to the memory to select the microinstructions for execution, the program counter responsive to logical outputs received from the macrocells.

6. The programmable logic device of claim **5**, wherein the program counter is responsive to a jump destination derived from a previously executed microinstruction.

7. The programmable logic device of claim **5**, wherein the memory is non-volatile.

8. The programmable logic device of claim **5**, wherein the microsequencer includes: a multiplexer having input terminals for receiving the logical outputs from the macrocells; an output terminal coupled to the program counter; and a select terminal coupled to an output terminal of the memory, the multiplexer responsive to a select command derived from a previously executed microinstruction.

9. A method of sequencing a finite state machine, comprising:

generating input conditions for a finite state machine in a programmable logic block based upon a set of inputs;

selecting an input condition from the generated input conditions based upon a previously-executed microinstruction selected from a hardwired read-only memory;

selecting a microinstruction from a set of stored microinstructions in the read-only memory based upon the selected input condition and the previously-executed microinstruction; and

executing the selected microinstruction to provide inputs for the set of inputs.

10. The method of claim **9**, wherein the selecting a microinstruction act comprises:

if the selected input condition is in a first binary state, selecting the microinstruction at a jump destination derived from the previously-executed microinstruction; and

if the selected input condition is complementary to the first binary state, selecting the microinstruction according to a predetermined microinstruction sequence.

11. The method of claim **10**, wherein the executing co the microinstruction act includes determining the first binary state.

12. The method of claim **9**, wherein the programmable logic block comprise a programmable AND array, and the generating input conditions act comprises processing product terms through the programmable AND array.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Edward A. Ramsden		
Assignee:	Lattice Semiconductor Corporation		
Title:	Programmable Logic Device With Hardwired Microsequencer		
Serial No.:	10/617,980	Filing Date:	July 10, 2003
Examiner:	Daniel Chang	Group Art Unit:	2819
Docket No.:	M-15145 US		

Irvine, California
February 23, 2005

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action dated November 29, 2004, Applicant submits the following amendments and remarks.

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

10. (original) The method of claim 9, wherein the selecting a microinstruction act comprises:

if the selected input condition is in a first binary state, selecting the microinstruction at a jump destination derived from the previously-executed microinstruction; and

if the selected input condition is complementary to the first binary state, selecting the microinstruction according to a predetermined microinstruction sequence.

11. (original) The method of claim 10, wherein the executing the microinstruction act includes determining the first binary state.

12. (original) The method of claim 9, wherein the programmable logic block comprise a programmable AND array, and the generating input conditions act comprises processing product terms through the programmable AND array.

13. (currently amended) A programmable logic device, comprising:

a logic block <u>including a plurality of macrocells, the macrocells</u> operable to provide input conditions for a finite state machine based upon a set of inputs; and

a hardwired microsequencer configured to determine a next state of the finite state machine by cyclically executing a

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049